REMARKS

Applicants note with appreciation the Examiner's indication that claims 1-20 are allowable. Applicants, however, submit the following comments regarding the Examiner's Reasons for Allowance stated on Page 2 of the Notice of Allowance. In the Reasons for Allowance, the Examiner indicated that the prior art of record fails to teach "the limitations of claim 18, lines 6-13: the removing portions of the dielectric layer to create covered portions and bare portions, the depositing of gate material, the doping of the first fin structure, source, and drain, with a first material and the second fin structure, source and drain with a second material, and removing a portion of the gate material over at least one covered portion."

This statement of reasons for allowance does not address the features recited in independent claims 1 and 12. Applicants note that each of claims 1, 12, and 18, independently, recite a combination of features not suggested or disclosed by the references of record. For example, claim 1 recites the following combination of features: "[a] method for forming a semiconductor device, comprising: forming a fin structure; forming a source region at one end of the fin structure; forming a drain region at an opposite end of the fin structure; forming an insulating layer in the fin structure, source region, and drain region, the insulating layer separating the fin structure into a first fin structure and second fin structure, the source region into a first source region and a second source region, and the drain region into a first drain region and a second drain region, the first fin structure, the first source region, and the first drain region being formed on an opposite side of the insulating layer of the second fin structure, the second source region, and the second drain region; forming a gate dielectric layer on surfaces of the first and second fin structures, the first and second source regions, the first and second drain regions,

and the insulating layer; removing portions of the gate dielectric layer to create covered portions and bare portions; depositing a gate material over the covered portions and bare portions; doping the first fin structure, the first source region, and the first drain region with a first material; doping the second fin structure, the second source region, and the second drain region with a second material; and selectively removing portions of the gate material to form the semiconductor device." The references of record do not disclose or suggest this combination of features.

Furthermore, claim 12 recites the following combination of features: "[a] method for forming a semiconductor device from a device that includes a first source region, a first drain region, and a first fin structure that are separated from a second source region, a second drain region, and a second fin structure by an insulating layer, the method comprising: forming an oxide layer over the device; removing portions of the oxide layer to create alternating covered portions and bare portions; depositing a gate material over the alternating covered portions and bare portions; doping the first fin structure, the first source region, and the first drain region with a first material; doping the second fin structure, the second source region, and the second drain region with a second material; and removing a portion of the gate material above the insulating layer and over at least one covered portion to form the semiconductor device." The references of record do not disclose or suggest this combination of features.

Applicants submit that it is the novel and non-obvious combination of features recited in each of claims 1, 12, and 18, independently, that distinguish these claims over the references of record.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

By: _____
John E. Harrity
Registration No. 43,367

Date: July 11, 2005

Harrity & Snyder, L.L.P.
11240 Waples Mill Road
Suite 300
Fairfax, Virginia 22030
(571) 432-0800